WHAT IS CLAIMED IS:

1. A high voltage transfer circuit, comprising:

a first high voltage switch for transferring a high voltage generated within a chip to the outside of the chip according to a clock signal and a first control signal; and

a second high voltage switch for transferring the high voltage generated outside the chip to the inside of the chip according to the clock signal and a second control signal.

2. The high voltage transfer circuit as claimed in claim 1, wherein the first high voltage switch comprises:

a first switch for transferring the first control signal to a first node;

a second switch for transferring the high voltage generated within the chip to a second node according to the potential of the first node;

a capacitor for controlling the potential of the second node according to the clock signal;

a third switch for transferring a voltage of the second node to the first node according to the potential of the second node; and

a fourth switch for transferring the high voltage generated within the chip to the outside of the chip according to the potential of the first node.

3. The high voltage transfer circuit as claimed in claim 1, wherein the second high voltage switch comprises:

a first switch for transferring the second control signal to a first node;

a second switch for transferring the high voltage generated outside the chip to a second node according to the potential of the first node;

a capacitor for controlling the potential of the second node according to the clock signal;

a third switch for transferring a voltage of the second node to the first node according to the potential of the second node; and

a fourth switch for transferring the high voltage generated outside the chip to the inside of the chip according to the potential of the first node.

4. A high voltage transfer circuit, comprising:

a pumping circuit for generating a high voltage necessary for an operation of a flash memory cell, and supplying the high voltage to an internal circuit;

a high voltage pad for receiving the high voltage generated from the pumping circuit, or the high voltage generated from the outside;

a first high voltage switch for transferring the high voltage generated from the pumping circuit to the high voltage pad according to a clock signal and a first control signal in a monitoring mode; and

a second high voltage switch for transferring the high voltage supplied to the high voltage pad from the outside to an internal circuit according to the clock signal and a second control signal in an external voltage supply mode.

5. The high voltage transfer circuit as claimed in claim 4, wherein the first high voltage switch comprises:

a first NMOS transistor driven by a power supply voltage, for transferring the first control signal to a first node;

a second NMOS transistor for transferring the high voltage generated within the chip to a second node according to the potential of the first node;

a capacitor for controlling the potential of the second node according to the clock signal;

a third NMOS transistor for transferring a voltage of the second node to the first node according to the potential of the second node; and

a fourth NMOS transistor for transferring the high voltage generated within the chip to the outside of the chip according to the potential of the first node.

6. The high voltage transfer circuit as claimed in claim 4, wherein the second high voltage switch comprises:

a first switch driven by a power supply voltage, for transferring the second control signal to a first node;

a second NMOS transistor for transferring the high voltage generated outside the chip to a second node according to the potential of the first node;

a capacitor for controlling the potential of the second node according to the clock signal;

a third NMOS transistor for transferring a voltage of the second node to the first node according to the potential of the second node; and

a fourth NMOS transistor for transferring the high voltage generated outside the chip to the inside of the chip according to the potential of the first node.